

REMARKS

Claims 1-26 have been presented for examination. Applicant would like to thank the Examiner for identifying the allowable subject matter.

Claim Rejections - 35 USC §103

Claims 1-6, 10-15, 17 and 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,574,240 ("Tzeng") in view of US patent application publication No. 2001/0049740 ("Karpoff"). Applicant respectfully traverses these rejections.

There are three basic criteria to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a). First, there must be some suggestion or motivation in the cited references to modify or combine their teachings; second, there must be reasonable expectation of success; and third, the prior art references must teach or suggest all the claim limitations. *See* M.P.E.P §2142. As to claim 11, the combination of cited references does not teach each and every limitation of claim 11.

As to claim 11, the Examiner has stated that Tzeng teaches "a plurality of transmitters (20) coupled to the L2/L3 switch (25) and a plurality of receivers (20) coupled to the L2/L3 switch (25) (See Fig. 1, Col. 3, lines 16-41)." (Emphasis added). Applicant respectfully point to the Examiner that claim 11 recites two distinct elements 1) a plurality of transmitters, and 2) a plurality of receivers; however, the Examiner has cited a single element 20 for transmitters and receivers. According to Tzeng, "[t]he MAC module 20 transmits and receives data packets to the associated network stations 14 across 10/100 Mbps physical layer (PHY) transceivers (not shown) according to IEEE802.3u protocol." (Col. 3, lines 31-34, emphasis added). Thus, there is only one module that performs the function of transmitting and receiving. In contrast, claim 11 recites plurality of transmitters and plurality of receivers, which is not taught by Tzeng. Therefore, the combination of cited references does not teach or suggest all the claim limitations. Accordingly, claim 11 is patentably distinguishable from the combination of cited references.

Claim 17 has been rejected in the manner of claim 11. Accordingly, claim 17 is patentably distinguishable from the combination of cited references for at least the same reasons as claim 11. Further as to claim 17, the Examiner has cited figure 5 of Tzeng as showing "a receive FIFO (51), a MAC queuing logic (52), a memory (53) (first means for receiving data ... MAC function)" and "a MAC dequeuing logic (54), a transmit FIFO (55), and a processor interface module (57) (second means for transmitting ... MAC function)" (Emphasis added). Applicants respectfully point to the Examiner that the means identified by the Examiner are actually part of a single means port filter 24. Furthermore, claim 17 has been amended to recite that the data transmission device includes a plurality of first and second means. The combination of cited references does not teach this limitation. Accordingly, claim 17 is further patentably distinguishable from the combination of cited references.

Claims 1-2, 17 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,574,240 ("Tzeng") in view of US patent application publication No. 2001/0049740 ("Karpoff") and US patent No. 5,892,768 ("Jeng"). Applicant respectfully traverses these rejections.

Claims 1 and 20-22 have been rejected in the manner of claim 11, accordingly, claims 1 and 20-22 are patentably distinguishable from the combination of cited references for at least the same reasons as claim 11. Further, the Examiner has cited Jeng; however, even citing Jeng, the Examiner has admitted that "Jeng in view of Tzeng and Karpoff teaches substantially all the claimed invention but did not disclose expressly the particular application involving limitations of separating the MAC (46) controls the RX path and MAC (48) controls the TX path from a single IC into two individual IC's." (Emphasis added). Thus, as the Examiner has also observed, the combination of Tzeng, Karpoff, and Jeng does not disclose every limitation of claims 1 and 20-22.

Further, the Examiner has stated that

It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate both the MAC (46) with receiver for the RX path and MAC (48) with transmitter for the TX path into a single IC for both same functions and less chip count as in the industrial design trend since it has been held by *In re Dulberg*,

289 F.2d 522, 523, 129 USPQ 348,349 (CCPA 1961). (Emphasis added)

Applicant respectfully points to the Examiner that in fact MAC 46 and MAC 48 are integrated in a single IC 44, which is part of the Ethernet port 40 (*see col. 3, lines 61-65*), and this is one of the aspects that distinguishes claims 1 and 20-22 from the combination of cited references. Accordingly, as the Examiner has also observed the distinction of claims 1 and 20-22, these claims are patentably distinguishable from the combination of cited references.

Claim 2 depends from claim 1 and is patentably distinguishable from the combination of cited references for at least the same reasons as claim 1. Further, regarding claim 2, the Examiner has stated that “Liang further teaches that PHY (28) ... “ (emphasis added). Applicants would like to respectfully point to the Examiner that in the current office action, the Examiner has not identified the Liang reference and have not provided any citations (e.g., patent number, publication number etc.) that the Applicants can use to review the reference.

Applicant respectfully requests that Examiner to identify the Liang reference or in alternative, withdraw the rejection of claim 2.

Claims 10 and 23 depend from claims 1 and 20 respectively, accordingly these claims are patentably distinguishable from the combination of cited references for at least the same reasons as claims 1 and 20. Further, regarding claims 10 and 23, the Examiner has stated that “Tzeng further teaches an integrated multiport switches (12) (hub) (See Fig. 1, Col. 3, lines 17-19), thus it is rejected with the same rationale applied against claim 11 above.” (Emphasis added). Applicants respectfully point to the Examiner that claims 10 and 23 recite that the device is part of a fiber node, a headend, a secondary hub, or a primary hub of a cable network. The cited reference does not teach and the Examiner has not identified a particular citation that teaches this limitation. Accordingly, these claims are further patentably distinguishable from the combination of cited references.

Regarding claim 12, the Examiner has stated that “Tzeng further teaches that data packets received at the fiber interface (16) are provided to the transmitters (20) without being read by the CPU ...” (Emphasis added). Applicant respectfully disagrees and points to the Examiner

that according to Tzeng, “[t]he host CPU 26 controls the overall operation of the corresponding switch 12, including programming of the switch fabric 25.” (Col. 3, lines 45-47). Accordingly, claim 12 is patentably distinguishable from the cited references.

Claims 3, 13, and 24 have been rejected using the same rationale as claim 12, accordingly, these claims are patentably distinguishable from the combination of cited references for at least the same reasons as claim 12.

Claims 4-6, 14-15, and 25 have been rejected in the manner of claims 1, 11, and 20. Accordingly, these claims are patentably distinguishable from the combination of cited references for at least the same reasons as claims 1, 11, and 20.

Applicant believes this application and the claims herein to be in a condition for allowance. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,



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